REMARKS

The Examiner rejected Claim 1-12 under 35 U.S.C. 101 stating that the claimed invention is directed to non-statutory subject matter. Applicant traverses the rejection.

The Examiner states that claims 1-12 are directed to non-statutory subject matter because they "merely disclose elements for performing mathematical function without disclosing a **practical application with a concrete, useful, and tangible result, as they are Pre-emptive in any application**". Although the claim recites the delivery of output bits from a register to a device external to the accumulator, the Examiner maintains that the "result produced by (the) claimed invention is merely (a) number" without "a real world value since the claimed invention is not for any practical application, and thus is not useful".

Applicant submits that the practical application of the current invention to signal processing is disclosed in the "Background of the Invention" section of the specification, on Page 1, lines 13-26. Moreover, the claim itself recites a device – a parallel digital accumulator – with specific structural components that operate to produce an output that can then be used by an external device. Furthermore, if the Examiner's argument were correct, no apparatus for performing a calculation would be patentable. In this regard, it should be noted that there are numerous patents granted to digital calculators. In fact, the existence of the Cox patent is evidence that the present invention is directed to patentable subject matter, since the output of the Cox device is a pure number having no real world value. Applicant submits that the current invention is indeed useful for practical applications in which high speed digital accumulators are desirable. Hence, Applicant submits that claim 1 and the claims dependent therefrom are not directed towards non-statutory subject matter.

The Examiner rejected claims 1-12 under 35 U.S.C. 103(a) as being clearly unpatentable over Cox, *et al* (hereafter "Cox"). Applicant submits that as currently amended, claims 1-12 are not unpatentable over Cox.

Claim 1 has been amended to make it clear that the speed at which the accumulator delivers the output bits to the external device is equal to the speed at which each adder in each of the plurality of partitions performs its adding function. Applicant submits that the specification of the current invention provides support for this amendment in the discussion of the arbitrary example of a 48-bit accumulator that operates at the speed of a 24-bit adder (Page 3, lines 25-28) and in the discussion of extending this feature to the case where each partition contains only a one-bit full adder and a one-bit register, in which limiting case the accumulator would operate at the speed of the one-bit adder (Page 3, line 30 – Page 4, line 2).

It should be noted that the clock period of the present invention is equal to the "half-cycle" defined in Cox. That is, the present invention provides two results in each of the cycles defined in Cox. Cox teaches (column 2, lines 29-44) a partitioned accumulator which operates to deliver output bits at a speed determined by the need for two "half-cycles" to occur for each accumulation operation. In the first half-cycle, an addition is performed on the least significant bits using the first two (low bit) adders 110, and, in the second half-cycle, an addition is carried out using the two high-bit adders 120. During the second half cycle, no addition takes place in the least significant partition. During the first half cycle, no addition takes place in the most significant partition. Hence, the effective operating speed of the accumulator of Cox is half the operating speed of the adders used within the accumulator partitions. The current invention improves on this prior art by doubling the operating speed of the accumulator relative to the cited prior art.

Hence, Applicant submits that claim 1 and the claims dependent therefrom are not unpatentable over Cox.

With respect to Claims 3-4, 7, 10, and 12, the Examiner admits that Cox does not teach the limitations in question. The Examiner attempts to overcome this problem by stating that the limitations are old and/or well known in the art, and hence, one would be motivated to add the features to the device of Cox because the device of Cox is a parallel accumulator. The mere fact that all of the elements of a claim are known to the art is not sufficient to sustain a rejection for obviousness. Identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. To establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference. The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. In addition, the teaching, motivation or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. Whether the rejection is based on an express or an implicit showing, there must be particular findings related thereto. In re Kotzab (CA FC) 55 USPQ2d 1313, 1316. Hence, Applicant submit that there are additional grounds for allowing 3-5, 7, 10, and 12.

Furthermore, with respect to Claim 12, in the apparatus taught in Cox, the output bits of the least significant partition identified by the Examiner, i.e., the output bits in register 130 are used in a further computation. The apparatus of Cox would not function if this were not the case. Hence, the alteration suggested by the Examiner would lead to a non-functional device. Accordingly, there are still further grounds for allowing Claim 12.

With respect to Claim 9, the Examiner points to registers S1 and S0 as the delay elements. However, these are the same elements that the Examiner identified as being the register of Claim 1. The registers in question are part of register 115. The claim requires that the delay elements are in addition to the registers. Hence, there are additional grounds for allowing Claim 9.

To aid the Examiner in understanding the differences between the Cox reference and the present invention, Applicant has attached hereto a schematic drawing of the Cox invention using the nomenclature of the present application.

Respectfully Submitted,

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